(12) UK Patent Application (19) GB (11) 2 215 913 (13) A

(43) Date of A publication 27.09.1989

(21) Application No 8900281.0

(22) Date of filing 06.01.1989

(30) Priority data
(31) 881556 (32) 15.02.1988 (33) KR

(51) INT CL⁴
H01L 27/10 29/92

(52) UK CL (Edition J)
H1K KGAM K1CA K1FL K11A3 K11C1A K11D K4C11 K4C14 K9B1 K9B1A K9C2 K9D1 K9N2 K9R2
U1S S2121

(56) Documents cited
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EP 0149799 A2 EP 0085988 A2

(58) Field of search
UK CL (Edition J) H1K KFL KGAM
INT CL⁴ H01L

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(54) Semiconductor memory device capacitor

(57) There is disclosed a memory cell comprising a semiconductor substrate (10) of first conductivity type for mounting integrated circuit elements, and a trench (12a, 12b) for forming a capacitor region extending vertically to the surface of said substrate. In the substrate region around the trench is formed a cell plate region (14) of second conductivity type for forming a charge storage region within said capacitor region. A high concentration semiconductor region (16) of the same conductivity type as said substrate is formed in the substrate region outside said cell plate region (14) to increase the charge stored in said capacitor region. A conducting material (18) stores charge responding to the voltage given within said trench. A dielectric layer (20) is formed between said conducting material (18) and said cell plate (14).

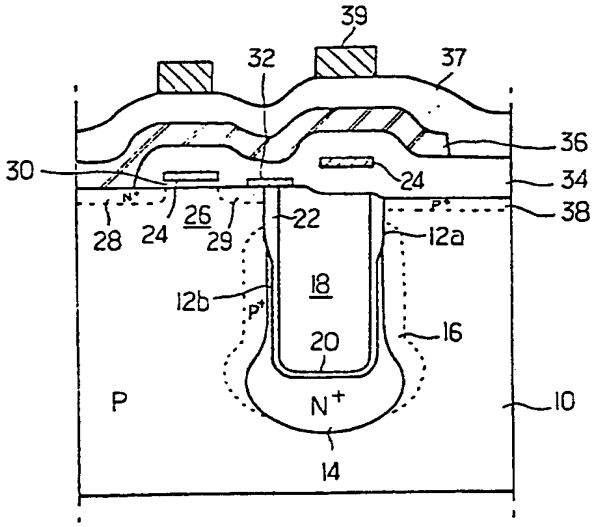

FIG. 1

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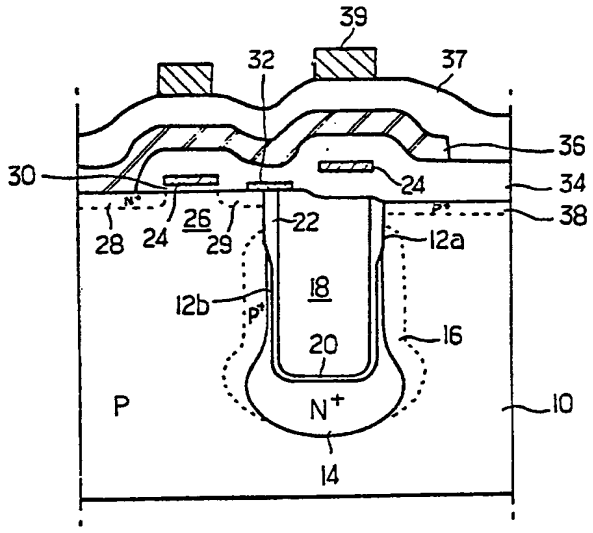

FIG. 1

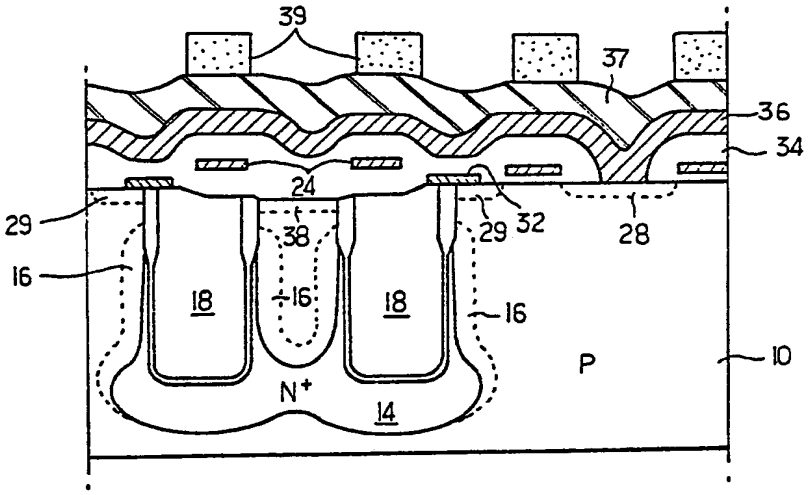

FIG. 2

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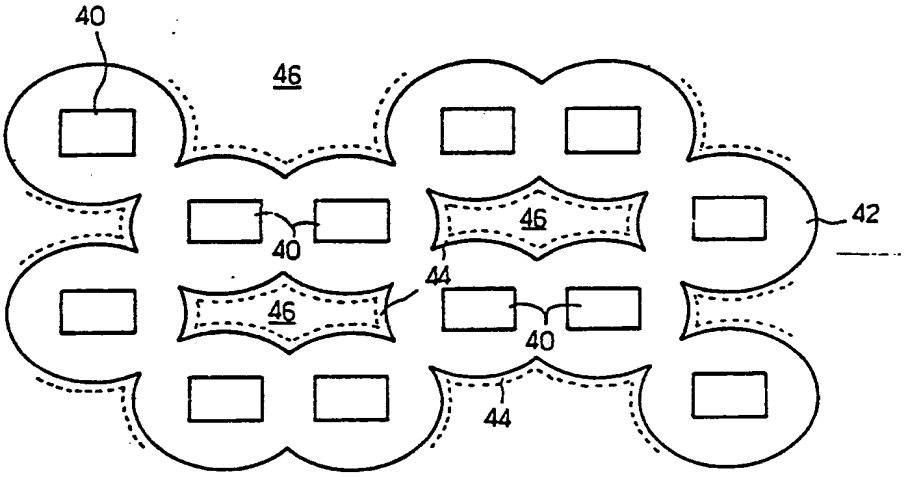

FIG. 3

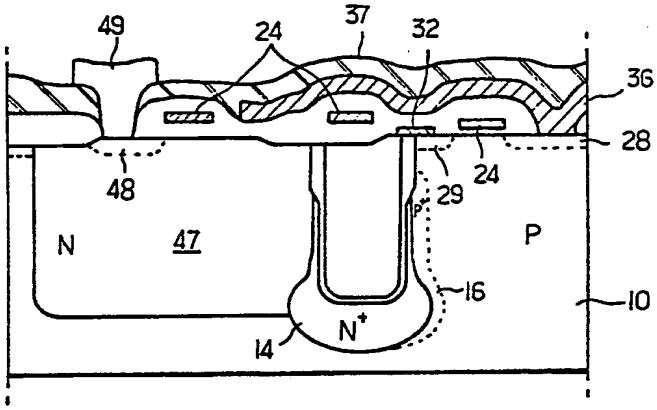

FIG. 4

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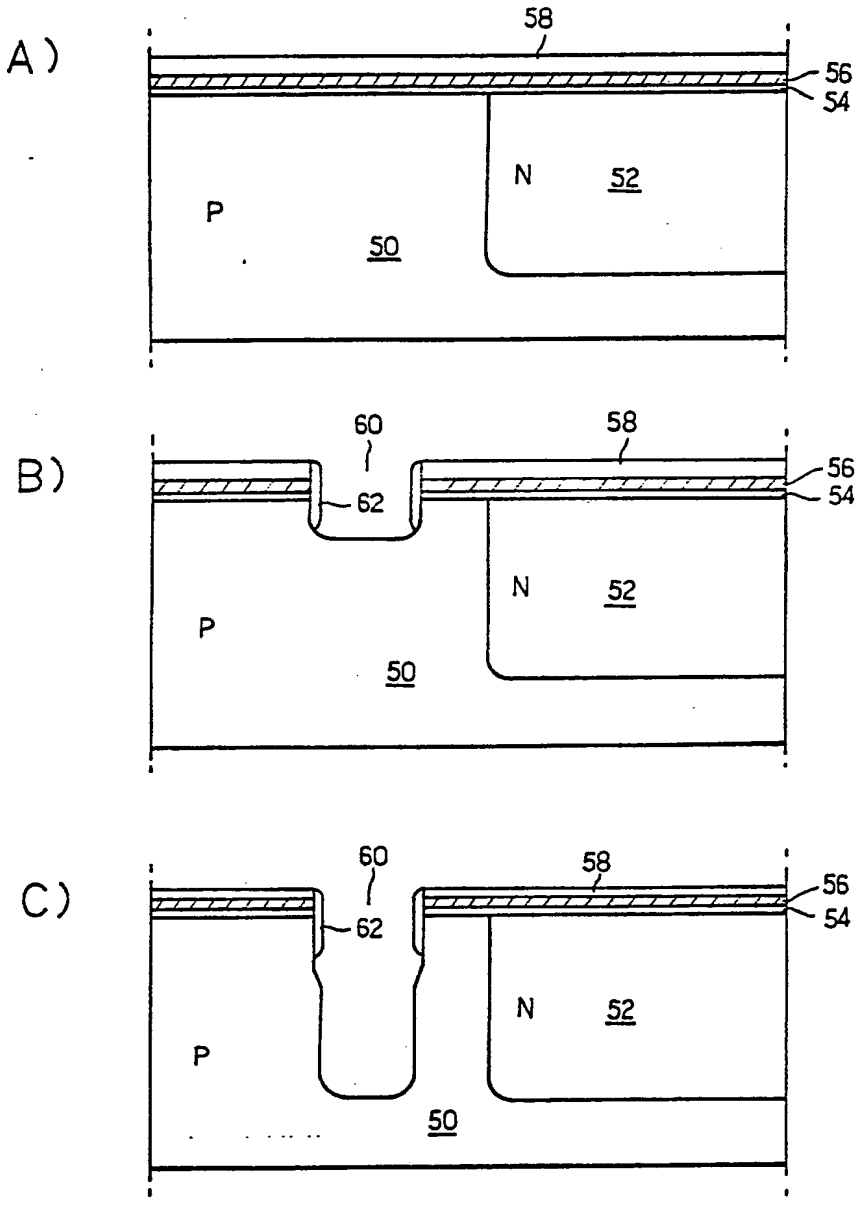

FIG. 5

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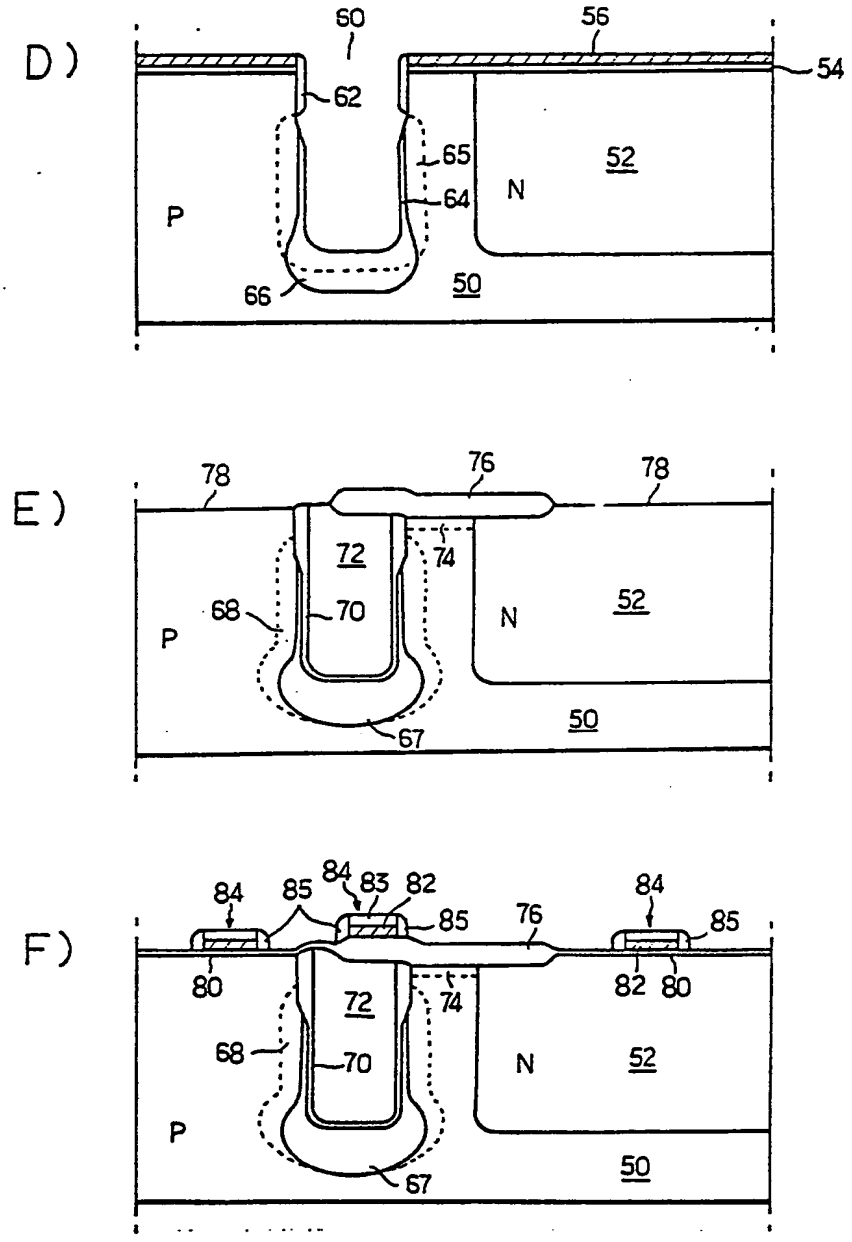

FIG. 5

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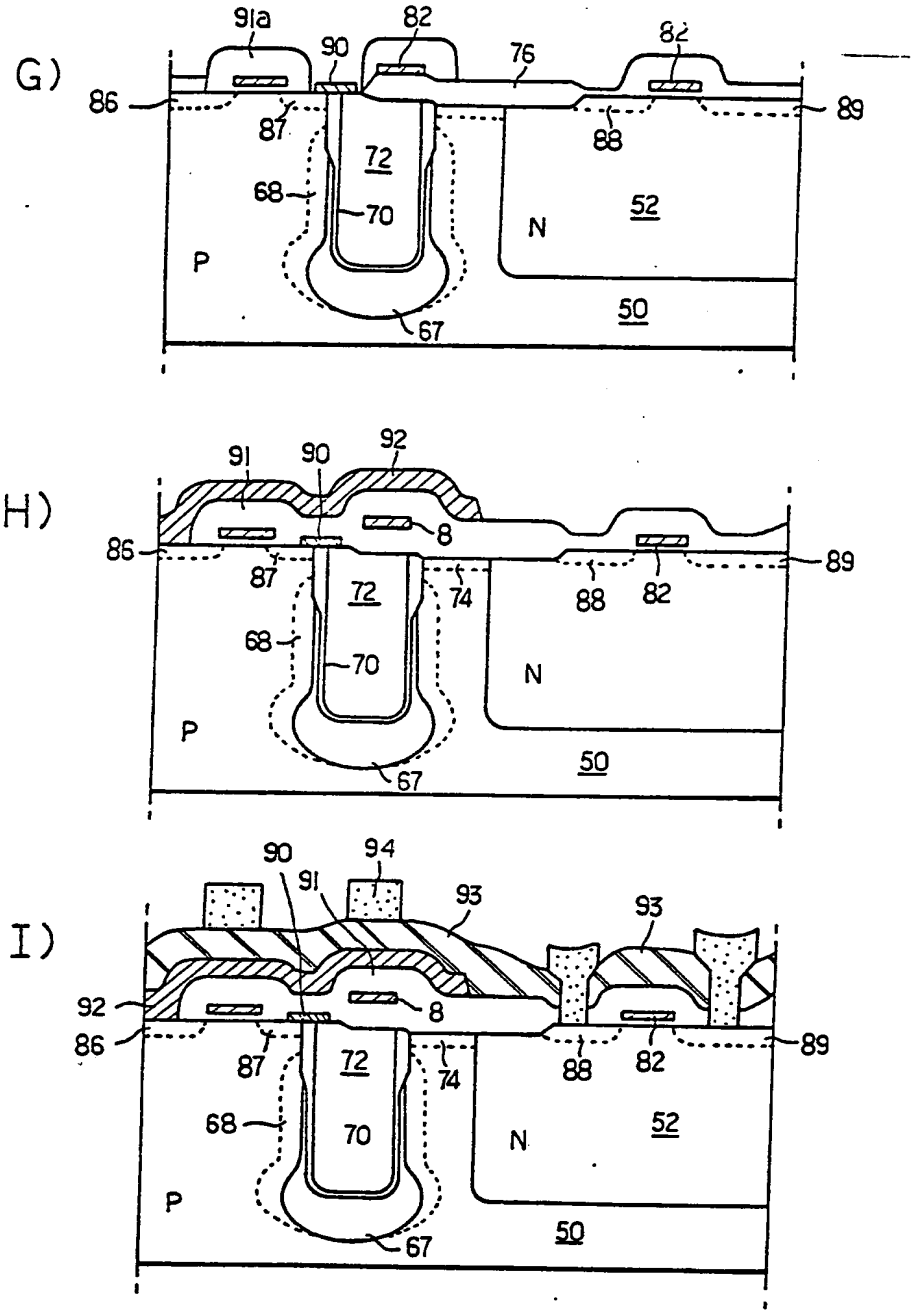

FIG. 5

SEMICONDUCTOR MEMORY DEVICE

The present invention relates to semiconductor memory devices, and is concerned particularly although not exclusively with a dynamic random access memory (DRAM) having a large capacity.

In the technical field of semiconductor memory devices, there have been many attempts to increase the memory capacity by increasing the number of memory cells on a single chip. In order to achieve such an object, it is important to minimize the area of the memory cell array by forming a plurality of memory cells on a limited surface of the chip, and in view of the minimum area it has been well known that a memory cell consisting of one transistor and one capacitor is desirable. However, since the capacitor occupies most of the area of the memory cell consisting of one transistor and one capacitor, it is important that though the area occupied by the capacitor is minimized, the capacitance thereof is increased so that the data reading operation is facilitated and the soft errors due to alpha α particles are reduced.

In order to resolve the above problem, there have been proposed several methods for forming capacitors comprising trenches on the surface of a semiconductor substrate so that the area occupied by the capacitor is minimized and the capacitance of the capacitor is maximized. In fact, it is necessary to employ such trench type construction in a DRAM having a storage capacity of more than four mega-bits.

An example of a memory cell employing a conventional tr nch construction is disclosed on pages

272-273 of ISSCC Digest of Technical Papers issued February, 1986.

Because the above memory cell has a cell plate of polysilicon formed on the upper surface of the substrate, the plate connection is difficult in a memory cell with a large integration of more than 16 kilo-bits, and the cell plate of polysilicon may easily produce step coverage which causes a stringer to be produced. Furthermore, as the above memory cell stores the charge outside the trench, soft error may easily be produced.

On the other hand, in a stacked memory cell forming a cell plate on word lines, the problem inherent in the above memory cell due to the plate may be resolved. However, if the trenches are formed in large integration, two adjacent trenches are separated from each other by a thick field oxide layer, so that the lower part of the field oxide layer cannot be effectively employed. Therefore, the degree of integration cannot be increased.

U.S. Patent Application No. 000743 filed on October 16, 1987 discloses a memory cell to solve the problems inherent in the above two types of memory cells. In the memory cell of U.S. Patent Application No. 000743, since the cell plate formed in the substrate has the same potential as the substrate, there cannot be independently applied to the cell plates a voltage different from that of the substrate.

Preferred embodiments of the present invention aim:

- to overcome the above drawbacks of the prior art and integrate a plurality of elements with high density, on a semiconductor substrate;

- to provide a memory cell comprising one transistor and one capacitor which, being fabricated with an allowable processing efficiency, has a cell plate submerged in the substrate, and enables a voltage different from that of the substrate to be applied to the cell plate.

- to provide a memory cell which is highly immune to noise and has a submerged cell plate; and/or

- to provide a memory cell having such a form and structure that can increase the fabrication efficiency.

More generally, according to one aspect of the present invention, there is provided a semiconductor memory device comprising at least one memory cell which includes a semiconductor substrate, at least one storage capacitor for storing charge in said semiconductor substrate, and a transfer transistor for transferring charges to said capacitor, said memory device comprising:

a trench formed in said substrate and extending to the surface of said substrate, said trench defining a region in which said capacitor is formed;

first dopant means forming a charge storing r gion in said capacitor region, said first dopant means being formed in the substrate around said trench;

second dopant means for increasing the charge stored in said capacitor region, said second dopant means being formed in the substrate region outside and adjacent to said first dopant means;

conducting means for storing the charge responding to the voltage given, said conducting means being formed in said trench;

dielectric means formed between said trench and said conducting means to serve as an insulator of said capacitor; and

connecting means for connecting said conducting means with said transfer transistor to transfer the charge to said capacitor region.

Preferably, said trench comprises a shallow trench portion opening into the surface of said substrate, the side walls of said trench portion being masked for preventing the penetration of dopants, and a deep trench portion formed continuously below said shallow trench portion, and said first and second dopant means comprise a fixed amount of impurities doped into the side walls of said deep trench.

Preferably, said shallow trench portion has a cross sectional area greater than that of said deep trench portion.

Preferably, said substrate and said second dopant means are of a first conductivity type and said first dopant means is of a second conductivity type. Preferably, said first conductivity type is P-type, and said s cond conductivity type is N-type.

The memory device preferably comprises an array of memory cells as aforesaid, at least one of which includes well means of the same conductivity type as said first dopant means and connected with said first dopant means of an adjacent memory cell.

Said adjacent memory cell is preferably at or adjacent one end of the array.

Said first dopant means of the adjacent memory cells are preferably connected with each other.

Such a memory device is preferably so arranged that a voltage of VCC/2 is applied to said well means, where VCC is the supply voltage to the memory device.

The memory is preferably constructed and arranged as a dynamic random access memory.

Preferably, said transfer transistor of the or each cell is a field effect transistor comprising a drain, source and gate.

Said trench preferably has side walls which extend substantially perpendicularly to the surface of said substrate.

Said conducting means of the or each cell preferably comprises a core of polysilicon disposed in the respective trench.

For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1 is a cross-sectional view of a one-transistor memory cell with a submerged storage capacitor according to a preferred embodiment of the present invention;

Figure 2 is a cross-sectional view illustrating the connection between two adjacent memory cells of the type shown in Figure 1;

Figure 3 is a plan view of part of a memory cell of the type shown in Figure 1;

Figure 4 is a cross-sectional view illustrating use of a memory cell of the type of Figure 1 to apply a voltage to a cell plate; and

Figs. 5(A)-(I) illustrate the processing steps in the fabrication of a one-transistor memory cell having a submerged storage capacitor.

In Figure 1, the reference numeral 10 indicates a P-type or N-type semiconductor substrate. Hereinafter, the description will be made for convenience with reference to the P-type substrate, but the inventive concept is equally applicable to the N-type substrate. A capacitor is formed in a trench having generally a tapering or conical shape, the inside of which trench is perpendicular to the surface of the semiconductor substrate. The trench comprises a relatively shallow and wide portion 12a, and a relatively deep and narrow portion 12b. In the peripheral area are formed an N+ cell plate region 14 highly doped with arsenic, phosphorus, etc. of opposite conductivity type to the substrat , and a P+ region 16 highly doped with boron, tc. of the same conductivity type as the substrate.

The N+ cell plate region 14 forms one electrode of the capacitor.

A hard polysilicon core 18 formed in the trenches 12a and 12b forms the other conducting electrode of the capacitor. This core 18 is isolated from the highly doped N+ cell plate region 14 by a dielectric layer 20 composed of oxide layer or a composition of the oxide and nitride. The thickness of the dielectric layer is approximately 100-200 Å.

The trenches are continuously formed by the process described below. During the first step of the process the shallow trench 12a is formed in the substrate by reactive ion etching. This shallow trench 12a extends approximately 1.5 μm into the substrate. When this shallow trench is formed, oxide layers are deposited on the inside and bottom thereof. Thereafter, once the bottom of the shallow trench is etched by using anisotropic etching, the whole oxide layer 22 remains on the inside wall of the trench so as to block the diffusion of impurities in a subsequent impurity diffusion process. In a second step of the process, the deep trench 12b having a thickness of about 3 - 3.5 μm is formed in the bottom of the shallow trench by etching. Impurities are introduced into the inside walls of the deep trench in order to form the highly doped N+ region and P+ region. At this time, the oxide layer 22 deposited on the inside walls of the shallow trench 12a serves as a barrier during the impurity diffusion process.

The transfer transistor comprises a gate 24, and drain and source regions 28 and 29 separated by a channel region 26 below the gate 24. The gate 24 and the

channel region 26 of the transistor are isolated from each other by a gate insulating layer 30 so as to limit the current flowing between the drain and source regions 28 and 29 in response to control signals applied to the gate 24. The source region 29 of the transistor and the polysilicon core 18 are connected with each other via a conducting polysilicon region 32 so as to transfer charges between the storage capacitor and the circuit for employing the charges. Insulating layers 34 and 37 cover various other layers on the semiconductor substrate, thereby protecting them. Conductors such as the conductor 36 formed so as to be connected with the drain region 28 of the transfer transistor serve to transfer the signals of the various elements. The conductor 39 is made of metal.

Figure 1 illustrates a cross section of the submerged storage capacitor. The P+ doping layer 38 below the insulating layer 34 is formed to reduce leakage currents between adjacent trenches. Furthermore, it is well known to those skilled in the art that the P+ region 16 outside the N+ cell plate region 14 isolates the N+ cell plate region 14 from the source region 29 of the transfer transistor to block leakage current, thereby serving to increase the capacitance of the storage capacitor.

Figure 2 is a cross-sectional view for illustrating the connections between adjacent cells, where the same reference numerals are used for the parts identical to those of Figure 1. As shown in Figure 2, adjacent cells are connected with each other via the N+ cell plate 14.

Figure 3 is the top view for illustrating a part of a memory cell array having the above structure. Numeral 40 indicates the trench region forming the capacitor, numeral 42 the N+ doped cell plate region, 44 the P+ doped region, and 46 the P-type substrate region. As shown in the drawing, the N+ cell plate regions (the region 14 in Figure 2) formed around the trench are connected to each other. At a specified terminal of the memory cell array there is provided a fixed voltage to the N+ cell plate region 42, which is illustrated in Figure 4. The same reference numerals are used to indicate the parts of Figure 4 identical to those of Figs. 1 and 2.

In an end portion of the memory cell array as shown in Figure 3 there is formed an N-well 47 as shown in Figure 4, to connect with the N+ cell plate region 14. On the upper part of the N-well 47 is formed an N+ doping layer 48 which is connected with a conductor 49. When a fixed voltage is applied to the conductor 49, it is supplied through the N-well 47 to the N+ cell plate 14. Hence, if the voltage is supplied to the N+ cell plate 14 connected with the N-well 47 due to the voltage applied to the N-well 47, all of the N+ cell plates 14 also receive the voltage because of their interconnections. It is preferable to apply a voltage of Vcc/2 (a half of the source supply voltage Vcc) to the N-well. If the cell plate 14 receives a reduced voltage of Vcc/2, the thickness of the insulating layer of the capacitor may be correspondingly reduced, thereby increasing the capacitance.

Hereinafter, with r ference to Figs. 5(A)-5(I) there will be xplained the steps of forming DRAM

cells on a silicon semiconductor substrate.

The starting material of silicon semiconductor wafer 50 is the N-type or P-type substrate, in which an N-well or P-well is formed by a conventional process of diffusion or ion implantation. The impurity concentration in the substrate of the well 52 formed at this time is about 10^{14} atoms/cm^3.

In the step of Figure 5A, the starting material is P-type silicon semiconductor substrate 50 having an N-well 52. At first, by conventional thermal oxidation there is formed an oxide layer 54 of SiO on the substrate 50 with a thickness of 200-400 Å. Then, a nitride layer 56 of Si_3N_4 and a thick oxide layer 58 are successively formed by a conventional process. The nitride layer 56 has the thickness of about 1000-2000 Å, and is used as an oxidation protecting mask in the subsequent process. The oxide layer 58 has a thickness of about 6000-8000 Å, is formed under low temperature, and is used as a mask during trench forming.

Thereafter, the oxide/nitride/oxide layers 54/56/58 are etched by photolithography to make an etching mask for forming the trench. Then, by reactive ion etching (RIE) the silicon substrate 50 is etched to form the trench 60. Subsequently, on the upper surface of the substrate and the surface of the trench 60 there are formed oxide layers having a thickness of 2000 Å by a conventional low temperature oxidation process, and the oxide layers are removed by etching without a separate mask on the bottom of an trench 60 and the surface of the substrate to form the oxide layer mask 62 on the inside walls of the trench 60 as shown in Figure 5(B). In the bottom of the

trench 60 there is then formed the deep trench by reactive ion etching as shown in Figure 5(C).

Referring to Figure 5(D), into the exposed side walls of the trench 60 except the portion covered with the oxidation mask 62, at an oblique angle, there are implanted P-type ions such as boron and N-type ions such as arsenic, respectively, at doses of 10^{12}-10^{13} ions/cm^2 and 10^{14}-10^{15} ions/cm^2, with an energy of about 50 KeV, so as to form the P-type semiconductor region 65 and N-type semiconductor region 64 on the substrate surface outside the trench. Then, the N-type semiconductor region 66 is formed in the substrate region below the bottom of the trench by N+ ion implantation or conventional diffusion process. The P-type semiconductor region 65 and N-type semiconductor region 64 may also be formed by a conventional diffusion process.

Referring to Figure 5(E), if the doping of the trench walls is completed as above, the dopants diffuse to form the N+ cell plate 67 and the P+ region 68. The N+ cell plate region 67 serves as an electrode of the capacitor. In order to make the capacitor insulating layer, a dielectric layer 70 comprising an oxide layer and/or nitride layer is formed on the side walls of the trench 60 and the surface of the substrate. The trench 60 is then filled with an N+ doping polysilicon core 72. The dielectric layer 70 and the doped polysilicon 72 are formed by a conventional process. The polysilicon core 72 stores charge, and forms one electrode of the capacitor. After removing the polysilicon on the nitride layer 56, and then the nitrid layer 56 and oxide layer 54 in the region for the field oxide layer, below this r gion is

formed a high concentration P-type doping region 74, and the field oxide layer 76 is subsequently grown. Thereafter, the nitride layer 56 and oxide layer 54 remaining an the substrate are all removed.

Referring to Figure 5(F), a gate oxide layer 80 is grown on the exposed substrate surface 78 by thermal oxidation, and a conducting polysilicon layer 82 and low temperature oxide layer 83 are formed on the entire surface of the substrate. The gate electrode pattern 84 is the formed by conventional photolithography. On the side walls of the gate electrode pattern 84 is formed an oxide spacer 85.

Referring to Figure 5(G), the N+ region as the drain and source regions 86 and 87 of an N-channel MOS field effect transistor (N-MOSFET) is formed on the substrate 50, and the drain and source regions 88 and 89 of a P-MOSFET are formed on the N-well 52. Then, an insulating layer 91a is coated with a low temperature oxide (LTO) or phosphor silicate glass (PSG), and there is formed a polycide connecting layer 90 by etching the connection area between the conducting polysilicon core 72 and the source region 87 of the N MOSFET as the transfer transistor. The source and drain regions of the MOSFET are formed by conventional phosphorus ion implantation. The submerged core 72 is connected with the transfer transistor through a thin conducting polysilicon layer formed by photolithography, or a silicide.

Referring to Figure 5(H), after coating an insulating layer by an LTO or PSG layer on the entire surface, a polysilicon layer 92 is formed on the insulating layer 91 to transfer the charge of the storage

capacitor, through making a contact window on the drain region 86 of the N-MOSFET.

Finally, referring to Figure 5(I), on the various elements of the semiconductor substrate 50 is formed a passivation layer. The N+ cell plate region 67 highly doped with N-type impurities serves as the cell plate of the trench capacitor. By the two step formation for doping the side walls and bottom of the trench 60 is formed the effective cell plate beneath the surface of the substrate 50, which achieves advantages.

The above described embodiment of the present invention provides a capacitor having a submerged cell plate usable for various integrated circuits such as one- transistor memory cell, etc. of DRAM. Of course, it will be easily appreciated by those skilled in the art that the present invention can variously be embodied without departing its scope. For example, the semiconductor substrate may be made of materials other than silicon. Also, the cell plate region and the region outside the cell plate having the opposite conductivity are doped highly with arbitrary P-type and N-type impurities, where boron, phosphorus and arsenic are listed only by way of example. Moreover, the cell plate region may be formed variously to give substantially the same effect without departing the spirit of the present invention. Therefore, the description made above with reference to the drawings is only an example of the present invention, and does not limit the scope of the invention.

As is appar nt from the above description, charge storage is mad in the polysilicon core 18 within

the trench rather than the inversion layer in the silicon substrate. Hence, charge leakage and punch-through phenomena are considerably reduced between the trenches and the other elements in the substrate, and the immunity to noises is increased by deterioration of alpha particles. Additionally, because the cell plate is formed beneath the substrate surface, problems are solved which appear during forming the cell plate on the substrate with polysilicon, and the process of photolithography therefor is omitted, thereby increasing productivity. Further, since it is possible to apply a separate voltage to the cell plate, the voltage of Vcc/2 may be applied to the cell plate, the capacitance may be increased by reducing the thickness of the capacitor dielectric layer, and productivity may be increased by reducing the depth of the trench. Moreover, since a high concentration layer of a conductivity opposite to that of the cell plate is formed around the cell plate, the capacitance of the capacitor is increased and the current leakage is prevented between the transfer transistor and the cell plate.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such f atures and/or steps ar mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. A semiconductor memory device comprising at least one memory cell which includes a semiconductor substrate, at least one storage capacitor for storing charge in said semiconductor substrate, and a transfer transistor for transferring charges to said capacitor, said memory device comprising:

a trench formed in said substrate and extending to the surface of said substrate, said trench defining a region in which said capacitor is formed;

first dopant means forming a charge storing region in said capacitor region, said first dopant means being formed in the substrate around said trench;

second dopant means for increasing the charge stored in said capacitor region, said second dopant means being formed in the substrate region outside and adjacent to said first dopant means;

conducting means for storing the charge responding to the voltage given, said conducting means being formed in said trench;

dielectric means formed between said trench and said conducting means to serve as an insulator of said capacitor; and

connecting means for connecting said conducting means with said transfer transistor to transfer the charge to said capacitor region.

2. A memory device as claimed in Claim 1, wherein said trench comprises a shallow trench portion opening

into the surface of said substrate, the side walls of said trench portion being masked for preventing the penetration of dopants, and a deep trench portion formed continuously below said shallow trench portion, and said first and second dopant means comprise a fixed amount of impurities doped into the side walls of said deep trench.

3. A memory device as claimed in Claim 2, wherein said shallow trench portion has a cross sectional area greater than that of said deep trench portion.

4. A memory device as claimed in Claim 1, 2 or 3, wherein said substrate and said second dopant means are of a first conductivity type and said first dopant means is of a second conductivity type.

5. A memory device as claimed in Claim 4, wherein said first conductivity type is P-type, and said second conductivity type is N-type.

6. A memory device according to any of Claims 1 to 5, comprising an array of memory cells as aforesaid, at least one of which includes well means of the same conductivity type as said first dopant means and connected with said first dopant means of an adjacent memory cell.

7. A memory device as claimed in Claim 6, wherein said adjacent memory cell is at or adjacent one end of the array.

8. A memory device as claimed in Claim 6 or 7, wherein said first dopant means of the adjacent memory cells are connected with each other.

9. A memory device as claimed in Claim 6, 7 or 8 so arranged that a voltage of VCC/2 is applied to said well means, where VCC is the supply voltage to the memory device.

10. A memory device according to any of Claims 1 to 9, constructed and arranged as a dynamic random access memory.

11. A memory device according to any of Claims 1 to 10, wherein said transfer transistor of the or each cell is a field effect transistor comprising a drain, source and gate.

12. A memory device according to any of Claims 1 to 11, wherein said trench has side walls which extend substantially perpendicularly to the surface of said substrate.

13. A memory device according to any of Claims 1 to 12, wherein said conducting means of the or each cell comprises a core of polysilicon disposed in the respective trench.

14. A semiconductor memory device substantially as hereinbefore described with reference to the accompanying drawings.

DOCKET NO: W&B-INF-1945
SERIAL NO:
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Published 1989 at The Patent Office, State House, 66/71 High Holborn, London WC1R 4TP. Further copies may be obtained from The Patent Office. Sales Branch, St Mary Cray, Orpington, Kent BR5 3RD. Printed by Multiplex techniques ltd, St Mary Cray, Kent, Con. 1/87